DIVISION/CONTINUATION APPLICATION TRANSMITTAL FORM

ATTORNEY'S DOCKET NO.
RD-26,616

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PRIOR APPLICATION:

EXAMINER	ART UNIT
K. PICARDAT	2822

To the Assistant Commissioner for Patents:

Transmitted herewith for filing is a ☐ continuation ☒ divisional application under 37 CFR 1.53 (b), of pending prior application

Serial No. 08/632,858 filed on April 16, 1996, of:

RAYMOND A. FILLION AND WILLIAM E. BURDICK

(Inventor)

For CHIP BURN-IN AND TEST STRUCTURE AND METHOD

(Title of Invention)

ENCLOSED ARE:

1. ☒ Specification having 18 total pages.

2. ☒ 9 sheets of ☒ formal ☐ informal drawings.

3. ☒ Declaration ☒ copy from prior application.
   ☐ newly executed (if additional inventor(s) under 37 CFR 1.63(d) (5).

4. ☒ Preliminary Amendment.

5. ☐ Signed statement deleting inventor(s) named in prior application under 37 CFR 1.63 (d) (2).

6. ☐ The power of attorney or correspondence address was was changed during prosecution of the prior application. A copy of the new power of attorney or correspondence address is submitted herewith under 37 CFR 1.63 (d) (4).

7. ☒ Other INFORMATION DISCLOSURE STATEMENT

The filing fee is calculated below:

	CLAIMS AS FILED IN THE PRIOR APPLICATION, LESS ANY CLAIMS CANCELED BY AMENDMENT BELOW			
	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE $760.00
TOTAL CLAIMS	7 - 20 =	0	X $18.00	$0.00
INDEPENDENT CLAIMS	2 - 3 =	0	X $78.00	$0.00
ADDITIONAL FEE FOR USE OF MULTIPLE DEPENDENT CLAIM(S) (once per application)			X $260.00	
		TOTAL FILING FEE		$760.00

(continued)

DIVISION/CONTINUATION APPLICATION TRANSMITTAL FORM

ATTORNEY'S DOCKET NO.
RD-26,616

8. ☒ Please charge $760.00 to my Deposit Account No. 07-0868.

9. ☒ The Assistant Commissioner is hereby authorized to charge all fees required under 37 CFR 1.16 or 1.17, or credit any overpayment to Deposit Account No. 07-0868.

10. ☒ Cancel in this application original claims 1-11 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

11. ☒ Amend the specification by inserting before the first line the sentence: This application is a ☐ continuation ☒ division of application Serial No. 08/632,858, filed 04/16/96, which is hereby incorporated by reference in its entirety.

12. ☐ Priority of application Serial No. _____ filed on _____ in _____ (country) is claimed under 35 U.S.C. 119.

☐ The certified copy has been filed in prior application Serial No. _____, filed _____.

SEND CORRESPONDENCE TO:

General Electric Company
CRD Patent Docket Rm 4A59
P.O. Box 8, Bldg. K1 - Salamone
Schenectady, New York 12301
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15 Dec 98
(date)

Signature ANN M. AGOSTI
Reg. No. 37,372

☒ attorney or agent of record

☐ Filed under §1.34(a)

Three copies of this form are enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on

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(Date of Deposit)

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Signature (Date of Signature)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
R.A. Fillion and W.E. Burdick

Applicant's Docket No. RD-26,616

For

CHIP BURN-IN AND TEST STRUCTURE AND METHOD

PRELIMINARY AMENDMENT

Honorable Commissioner of Patents and Trademarks,
Washington, DC 20231

S I R:

Prior to examination, please amend this application as follows.

In the title, please delete "AND METHOD."

In the claims, please amend claim 12 and add claims 14–17 as follows.

12. A burn-in fixture comprising:

burn-in frame having at least one window and including resistors having resistor pads;

at least one integrated circuit chip having chip pads and situated in the at least one window;

a flexible layer attached to the burn-in frame and the at least one integrated circuit chip, the flexible layer having via openings extending to the chip pads and the resistor pads; and

a pattern of electrical conductors extending over the flexible layer and extending into the vias [; and

means for burning in the at least one integrated circuit chip].

14 (new). The fixture of claim 12 wherein the burn-in frame comprises a ceramic or an insulated metal.

15 (new). The fixture of claim 14 wherein the flexible layer comprises a polymer.

16 (new). An electronic device package comprising:

an integrated circuit chip having chip pads on a top surface;

a flexible layer overlying the integrated circuit chip, the flexible layer having via openings extending to the chip pads; and

a pattern of electrical conductors extending over portions of the flexible layer and into the via openings and forming a reconfigured universal array of test and interconnection pads on the flexible layer,

the integrated circuit chip, the flexible layer, and the pattern of electrical conductors forming a known good electronic device package.

17 (new). The device in claim 16 wherein the flexible layer includes at least one resistor and wherein the pattern of electrical conductors couples the at least one resistor to at least one of the test and interconnection pads.

18 (new). The device of claim 16 wherein the flexible layer comprises a polymer.

REMARKS

Approval of the amendments is respectfully requested.

Respectfully submitted,

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RD-26,616 IS A DIVISION OF RD-24,889

CHIP BURN-IN AND TEST STRUCTURE AND METHOD

BACKGROUND OF THE INVENTION

The widespread use of multichip module (MCM) technologies has been inhibited by the poor yield and infant mortality of untested and unburned-in bare chips. Whereas a single chip package approach has a packaged part yield equal to that of the product of the assembly yield and the chip yield, multichip approaches have packaged part yields equal to the product of the MCM assembly yield and each of the chip yields. A single chip package with an assembly yield of 95% and a die yield of 95% has a package yield of just over 90%. A four chip MCM with the same assembly and die yields has a package yield of less than 80%, and an eight chip MCM with similar yields has a package yield of about 60%. In MCM designs for which rework is impractical, higher final package yields are required and can only be achieved with higher chip yields.

Infant mortality failures create similar concerns. For single chip packaging, individual packaged parts can be burned-in, i.e., powered with active or passive signals on each component I/O (input/output) pad at an elevated temperature to accelerate a significant percentage of latent chip defects that can be identified prior to component use. Bare chips are generally not subjected to burn-in testing prior to use in a multichip assembly.

Growth of the multichip module (MCM) market is thus limited by a lack of low cost known good die (KGD). KGD are singulated die (bare chips) tested and verified to the manufacturer's specification. KGD are functionally equal to packaged counterparts but have significantly higher costs.

Currently, KGD have been cost effective only for the most demanding MCM designs.

High density interconnect (HDI) is a high performance chip packaging technology wherein sequential layers of metallization on polymer are used to interconnect chip pads with high chip density, controlled impedance, and the elimination of the need for solder bump, wirebond, or TAB (tape automated bond) processing. In one form of HDI circuit module, an adhesive-coated polymer film overlay having via openings covers a plurality of integrated circuit chips in chip wells on an underlying substrate. The polymer film provides an insulated layer upon which is deposited a metallization pattern for interconnection of individual circuit chips through the vias. Methods for performing a HDI process using overlays are further described in Eichelberger et al., U.S. Pat. No. 4,783,695, issued Nov. 8, 1988, and in Eichelberger et al., U.S. Pat. No. 4,933,042, issued Jun. 12, 1990. Multiple layers of polymer overlays and metallization patterns are typically applied.

Cole et al., "Fabrication and Structures of Circuit Modules with Flexible Interconnect Layers," U.S. Application No. 08/321,346, filed October 11, 1994, describes a method for fabricating a circuit module using a flexible interconnect layer including a metallized base insulative layer and an outer insulative layer. At least one circuit chip having chip pads is attached to the base insulative layer and vias are formed in the outer and base insulative layers to expose selected portions of the base insulative layer metallization and the chip pads. A patterned outer metallization layer is applied over the outer insulative layer extending through selected ones of the vias to interconnect selected ones of the chip pads and selected portions of the base insulative layer metallization. Because

of the metallized layer on the flexible interconnect layer, the number of overlays necessary to achieve the desired interconnections can be reduced and thus the volume and weight of a circuit module can be lowered.

SUMMARY OF THE INVENTION

It would be desirable to have a technique for low cost burn-in and test of integrated circuit chips.

In the present invention, testing and burn-in can be performed using a high density interconnect process on a frame having windows and populated with logic and power components. The processing can provide chip pad reconfiguration to satisfy post test and burn-in chip attach requirements. Furthermore, the processing can be used to eliminate the need to redesign second level assembly printed circuit boards (PCBs) through the use of a discretionary interconnect approach which will accommodate a change in chip geometry or pad layout which can result from chip shrinkages or substitutions of chips from different chip manufacturers.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, where like numerals represent like components, in which:

FIG. 1 is a top view of a frame of the present invention.

FIG. 2 is a more detailed top view of a portion of the frame of FIG. 1.

FIG. 3 is a top view of a portion of a frame surrounding an integrated circuit chip.

FIG. 4 is a top view similar to that of FIG. 3 and further showing interconnections between chip pads and the frame.

FIG. 5 is a top view of the integrated circuit chip of FIG. 4 after removal from the frame.

FIG. 6 is a sectional side view along line 6-6 of FIG. 5.

FIG. 7 is a top view of a frame surrounding two chips.

FIG. 8 is a sectional side view along line 8-8 of FIG. 7.

FIG. 9 is a top view of a frame surrounding a multichip module.

FIG. 10 is a sectional side view along line 10-10 of FIG. 9

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

FIG. 1 is a top view of a frame 10 of the present invention including windows 12 and frame connection pads 14. The frame preferably comprises a material capable of withstanding a desired burn-in environment such as bake cycles of 100 °C, 125 °C, and 150 °C, for example. Such material may include ceramics such as fired ceramics, co-fired ceramics, glass ceramics, alumina, aluminum nitride, and beryllium oxide; insulators on metals such as porcelain, polymer, or diamond film on steel, titanium, or metal matrix composites; metal; metal matrix compositions; or glass/polyimide. The frame has one or more openings that

surround a chip (shown in FIG. 3) or multiple chips. In a preferred embodiment, the frame is designed to be reusable.

FIG. 2 is a more detailed top view of a portion of the frame of FIG. 1 which shows resistors 16 having resistor pads 16a, fuses 18 having fuse pads 18a, a signal track 21, and voltage bias tracks 20 and 22. For simplicity of illustration, resistor pads 16a are shown for only one resistor in FIG. 2. In one embodiment, the frame of FIG. 2 is attached to a flexible layer (shown in FIG. 6) with an adhesive prior to the insertion of any integrated circuit chips in frame windows 12. The adhesive may comprise, for example, a laser-abatable material such as an SPI (siloxane polyimide)-epoxy blend such as disclosed in Gorczyca et al., U.S. Pat. No. 5,161,093, issued Nov. 3, 1992.

Burn-in load resistors and fuses can be situated within or on the surface of frame 10. Typical burn-in networks require a protection resistor connecting each chip input signal pad (or group of input signal pads) and each output signal pad to a respective selected voltage potential or to a respective active (changing) logic level. In addition, current limiting fuse elements can be connected to chip power and ground pads. Resistors 16 may comprise thick film or thin film fired resistor pastes, other thin film deposited materials, discrete resistors, or resistor arrays.

If desired, fuses can be omitted or incorporated into the flexible layer. For example, a narrow metal trace will separate and act as a fuse if a high enough current is applied for a sufficient amount of time. The flexible layer can also contain some resistor elements fabricated either prior to attaching the frame or during interconnect processing after the chips are attached.

FIG. 3 is a top view of a portion of a frame surrounding an integrated circuit chip 24 having chip pads

26. In one embodiment, frame 10 is attached resistor side down to the flexible layer, and each integrated circuit chip is attached chip pad side down to the flexible layer through frame windows 12 with an adhesive such as an SPI-epoxy. In another embodiment, the chips can be attached to the flexible layer prior to the addition of frame 10. Frame 10 can then be attached so that the windows appropriately surround the chips. In yet another embodiment, chips can be positioned in frame windows that extend only partly through the frame, and the flexible layer can be applied to the frame and chips simultaneously. This embodiment can provide a heat sink for the chips which is particularly useful for high power chips. This embodiment also offers protection of the back side of the chips during the processing and burn-in. The process of attaching the chips in the windows can include using a chip attach material that is removed with a solvent. The chip attach material can include materials having a softening temperature about twenty to thirty degrees less than the softening temperature of adhesive between the chip and the flexible layer. Cole et al., U.S. Pat. No. 5,434,751, issued July, 18, 1995 describes a solvent soluble release layer comprising materials such as soluble polyimides, acrylics, polysulfones, polyesters, and blends, for example. The frame and chip removal requirements of this embodiment cause it to be more costly than the other embodiments.

Electrical connection areas for coupling to external biases and signals can be made from either the frame or metallization on the flexible layer. Frame connections can be made, for example, with edge contact fingers (shown as frame contacts 14 in FIG. 1) or connector pins. These external connection areas can then be inserted into conventional burn-in sockets, for example, for burn-in after

the frame and chip interconnections have been formed as discussed below.

FIG. 4 is a top view similar to that of FIG. 3 and further showing interconnections between chip pads and the frame; **FIG. 5** is a top view of the integrated circuit chip of FIG. 4 after removal from the frame; and **FIG. 6** is a sectional side view along line 6-6 of FIG. 5.

Flexible layer 34 (shown in the side view of FIG. 6) may comprise an insulating material upon which an electrically conductive material can adhere. Appropriate materials, for example, include polymers such as polyimides. The flexible layer may additionally comprise, if desired, a patterned metallization layer (shown as layer 29 in FIG. 8) on one or both surfaces of the insulating material. In one embodiment, the metallization layer comprises a metal adhesion-promoting seed material such as titanium or $SnCl_2$, followed by an electrolessly applied layer such as copper which can be coated by a thicker electroplated metal layer such as copper.

After the flexible layer is situated adjacent the chips and frame, via openings in the flexible layer extending to the chip pads and the resistors are provided by any appropriate process. A preferred method of laser-drilling vias in a polymer film is described in Eichelberger et al., U.S. Pat. No. 4,894,115, issued Jan. 16, 1990.

Next a pattern of electrical conductors 28 can be applied over the flexible layer and into the vias. Preferably the pattern of electrical conductors includes test and/or reconfiguration pads 30 situated over the flexible layer. In one embodiment, the pattern of electrical conductors 28 can be deposited by sequentially sputtering a thin layer of titanium (for adhesion purposes), sputtering a thin layer of copper, and electroplating a thicker layer of copper

(typically ranging from three to ten micrometers). Pads 30 can be deposited by sputtering a material such as gold, palladium, or nickel gold, for example, which will meet the particular application's requirements. Pattern of electrical conductors 28 and pads 30 can be patterned with photoresist to provide the desired connections and pads. As shown in FIG. 4, portions 28a couple chip pads 26 to bias tracks 20 and 22; portions 28b couple chip pads to resistor pads 16a; portions 28c couple chip pads to fuse pads 18a; portions 28d couple resistors to bias or signal tracks; portions 28e couple fuses to bias tracks; and portions 28f couple chip pads to test or reconfiguration pads 30. The bias and signal tracks can extend to frame connection pads 14 which preferably comprise a gold or other noble metal.

The pattern of electrical conductors and/or a patterned metallization layer of a flexible layer can fan-out the chip pads to an array of testable pads located at the flexible layer perimeter or fan-in (as shown) the chip pads 30 to a readily testable pad configuration located within the perimeter of each chip. If pad reconfiguration for the final die package is desired, the fan-in test pad configuration can simultaneously satisfy both the test and second level assembly requirements.

One of the challenges of any burn-in and test process is providing for the number of I/O (input/output) chip pads used in standard burn-in and test systems. In the present invention, the burn-in connections can be made in parallel to I/O chip pads with common functions with the burn-in being accomplished through frame connection pads 14, and a second set of pads 30 can be situated, preferably in the window region, to provide for testing and layout reconfiguration.

Test pads are used to couple chip pads, including input, output, and bias pads, to input, output, and bias test pins of an electronic test system. Generally, each chip pad must be connected separately to a separate test pad, and thus chip pads are not electrically connected together during electrical testing.

Many conventional approaches to burn-in require one burn-in contact per chip pad. In the present invention, the pattern of electrical conductors 28 can connect a plurality of input chip pads together and through a protective resistor to a bias or logic signal; connect each chip output pad to a bias or a logic signal through a protection resistor; and connect each chip bias pad through a current triggered fuse or directly to the bias busses. Thus, in the present invention, burn-in is permitted with only a few bias contacts to frame connection pads.

Because of the interconnect density, each frame can be populated with many chips, each having a large number of I/O chip pads. For the case of a frame with a usable flexible layer area of thirty to forty square inches, several hundred chips could be simultaneously processed through burn-in and test. Standard burn-in only systems utilize parallel connections to reduce the number of burn-in I/O contacts, however, they must rely on multiple layer burn-in boards populated with expensive burn-in sockets including a socket pin per chip contact.

In the case of bare chips, such as silicon integrated circuit chips, the devices are unpackaged and do not have robust contact pins. Instead, bare chips have chip input and output pads that are typically four mils by four mils of thin (one to two microns) aluminum. The aluminum pads generally develop a surface oxide layer that impedes electrical contact. Cost effective, reusable test sockets

for high temperature burn-in that do not damage the chip input and output pads are not readily available. Similarly, electrical testing of bare chips requires either probe contacts that damage chip pads or requires expensive bare chip sockets that typically involve excessive manual handling, have poor electrical contacts, and can cause chip damage during handling.

An added expense to standard burn-in systems is the need to remove chips from burn-in boards and install them in test boards to electrically isolate the chips prior to test. This expense does not occur with the present invention. In the present invention, the chips can be electrically isolated by removal of the parallel burn-in connections if they are situated on a disposable portion of the flexible layer. The removal of the burn-in connections can be performed by mechanical techniques, chemical etching, or laser ablation, for example. Once electrically isolated, the test pads can be used for testing without a need for extra handling or a test socket.

Once functionally verified, each chip can be excised from the frame by means of a laser, mechanical punch, water jet, or other precision cutting device. After removal, the flexible layer overlying the chip can remain in position, if desired, and thereby result in a fully tested and burned-in KGD with pads reconfigured as desired and the die surface protected from mechanical damage. This chip scale packaged chip could be directly attached to a PCB, or MCM without need for additional processing.

The pad 30 reconfiguration can be used to convert I/O chip pads from manufacturer unique to universal pad locations and modified to make possible equivalent functionality by substitution of chips from different manufacturers. Each reconfiguration option and process

would require a simple and inexpensive change in the chip to interconnect layout, which is unique to each design and located within the boundaries of the chip perimeter. The frame would not require any redesign as a result of a change in I/O chip pad reconfiguration. Therefore, changes in chip pad locations, chip manufacturers, and/or second level assembly requirements do not create the need to redesign burn-in and test hardware.

An option of the present invention is to apply solder 33 to reconfigured pads 30 after burn-in and testing and before each chip is removed from the frame. An inexpensive method of solder application is screen or stencil printing wherein a solder paste is applied to openings in the screen or stencil to desired pad locations using a squeegee. The application can be performed conveniently on a large area such as a wafer, panel, or board and is less costly and time intensive than individually applying solder to pads. Solder applied prior to burn-in can soften and reflow and thus distort the solder form. Electrical testing to solder control pads is not desirable because of the non-planar surface of the solder and the damage that test contacts can cause to the solder. A useful solder paste material 33 for application to pads 30 is a tin/lead eutectic solder. After application of the solder, the frame can be subjected to a standard solder reflow cycle which typically includes baking the frame to drive out any volatile substances from the solder paste and thermally exposing the frame to a temperature sufficient to reflow the solder into a solid solder contact ball that can later be used to attach the chip to a printed circuit board.

FIG. 7 is a top view of two chips 24 and 124 each having chip pads 26 and 126, respectively, and situated within a single frame opening 12, and **FIG. 8** is a sectional

side view along line 8-8 of FIG. 7. The positioning of two or more chips within a common frame window increases the number of components that can be incorporated into a fixed frame area. FIG. 8 further illustrates a patterned metallization layer 29 on flexible layer 34.

FIG. 9 is a top view of a frame window surrounding two chips 324 and 424 (having module pads 326 and 426, respectively) that are configured to form a multichip module 323, and **FIG. 10** is a sectional side view along line 10-10 of FIG. 9. In this embodiment, the flexible layer and pattern of electrical conductors can be used to interconnect the two chips as shown in FIG. 9 by portion 28g of pattern of electrical conductors 28 in addition to providing the electrical interconnections for performing burn-in and providing reconfiguration/test pads.

In another embodiment, the chips in a multichip module are already interconnected prior to being attached to flexible layer 34. In this embodiment, the "module pads" comprise electrically conductive connection pads or portions of electrically conductive material on the multichip module.

In the embodiment of FIG. 10, metallization layers 29 are present on both sides of flexible layer 34, so an additional flexible layer 31 is applied over flexible layer 34 prior to the addition of pattern of electrical conductors 28. Additional flexible layer 31 may be applied in any appropriate manner such as lamination, spray coating, or spin coating, for example, and may comprise a material similar to that of flexible layer 34.

Multichip module 323 includes a substrate 25. Chips 324 and 424 can be positioned in the substrate prior to being attached to flexible layer 34, or, substrate molding material can be applied to surround the chips after being

attached to flexible layer 34 in a similar manner as described with respect to Fillion et al., U.S. Pat. No. 5,353,498, issued Oct. 11, 1994. The process of applying molding material can also be useful when a single chip is present in a window because the molding material can help to protect the chip during processing.

While only certain preferred features of the invention have been illustrated and described herein, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

WHAT IS CLAIMED IS:

1. A burn-in method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors with resistor pads;

situating at least one integrated circuit chip having chip pads in the at least one window;

forming via openings in the flexible layer extending to the chip pads and the resistor pads;

applying a pattern of electrical conductors over the flexible layer and extending into the vias; and

burning in the at least one integrated circuit chip.

2. The method of claim 1, wherein the burn-in frame further includes fuses having fuse pads and the step of forming via openings includes forming via openings extending to the fuse pads.

3. The method of claim 2, wherein the burn-in frame further includes bias tracks and the step of forming via openings includes forming via openings extending to the bias tracks.

4. The method of claim 1, wherein the step of situating the burn-in frame occurs prior to the step of situating the at least one integrated circuit chip.

5. The method of claim 1, wherein the step of applying the pattern of electrical conductors includes applying a pattern of electrical conductors including test pads situated over the flexible layer.

6. The method of claim 5, further including the steps of after burning in the at least one integrated circuit chip, electrically isolating the chip pads and testing the at least one integrated circuit chip through the test pads.

7. A burn-in method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors having resistor pads;

situating at least one multichip module having module pads in the at least one window;

forming via openings in the flexible layer extending to the module pads and the resistor pads;

applying a pattern of electrical conductors over the flexible layer and extending into the vias; and

burning in the at least one multichip module.

8. The burn-in method of claim 7, wherein the step of situating the at least one multichip module comprises situating a plurality of chips having chip pads and a common substrate in the at least one window and the module pads comprise chip pads, prior to coupling the chip pads;

wherein the step of applying pattern of electrical conductors over the flexible layer includes coupling the chip pads by applying a pattern of electrical conductors that couples selected chip pads of the plurality of chips.

9. The method of claim 7, wherein the step of applying the pattern of electrical conductors includes applying a pattern of electrical conductors including test pads situated over the flexible layer and further including the steps of after burning in the at least one multichip

module, electrically isolating the chip pads and testing the at least one integrated circuit chip through the test pads.

10. A burn-in and test method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors having resistor pads, fuses having fuse pads, and voltage bias tracks;

situating at least one integrated circuit chip having chip pads in the at least one window and on the flexible layer;

forming via openings in the flexible layer extending to the chip pads, the resistor pads, the fuse pads, and the voltage bias tracks;

applying a pattern of electrical conductors over the flexible layer and extending into the vias, the pattern of electrical conductors including test pads situated over the flexible layer;

burning in the at least one integrated circuit chip;

electrically isolating the chip pads; and

testing the at least one integrated circuit chip through the test pads.

11. The method of claim 10, wherein the step of applying the pattern of electrical conductors includes positioning the test pads so as to reconfigure a chip pad layout, and

further including, after burning in and testing the at least one integrated circuit chip, applying a pattern of solder paste to the test pads and reflowing the solder paste into a solid solder contact.

12. A burn-in fixture comprising:

burn-in frame having at least one window and including resistors having resistor pads;

at least one integrated circuit chip having chip pads and situated in the at least one window;

a flexible layer attached to the burn-in frame and the at least one integrated circuit chip, the flexible layer having via openings extending to the chip pads and the resistor pads;

a pattern of electrical conductors extending over the flexible layer and extending into the vias; and

means for burning in the at least one integrated circuit chip.

13. The fixture of claim 12, wherein the burn-in frame further includes fuses having fuse pads and voltage bias tracks, and wherein the via openings extend to the fuse pads and voltage bias tracks.

CHIP BURN-IN AND TEST STRUCTURE AND METHOD

ABSTRACT

A burn-in frame having at least one window and including resistors having resistor pads is situated on a flexible layer, and at least one integrated circuit chip having chip pads is situated in the at least one window. Via openings are formed in the flexible layer to extend to the chip pads and the resistor pads. A pattern of electrical conductors is applied over the flexible layer and extending into the vias. The at least one integrated circuit chip is burned in. The burn-in frame may further include fuses, frame contacts, and voltage bias tracks. After burning in the at least one integrated circuit chip, the chip pads can be electrically isolated and the at least one integrated circuit chip can be tested. This method can also be used to burn-in and test multichip modules.

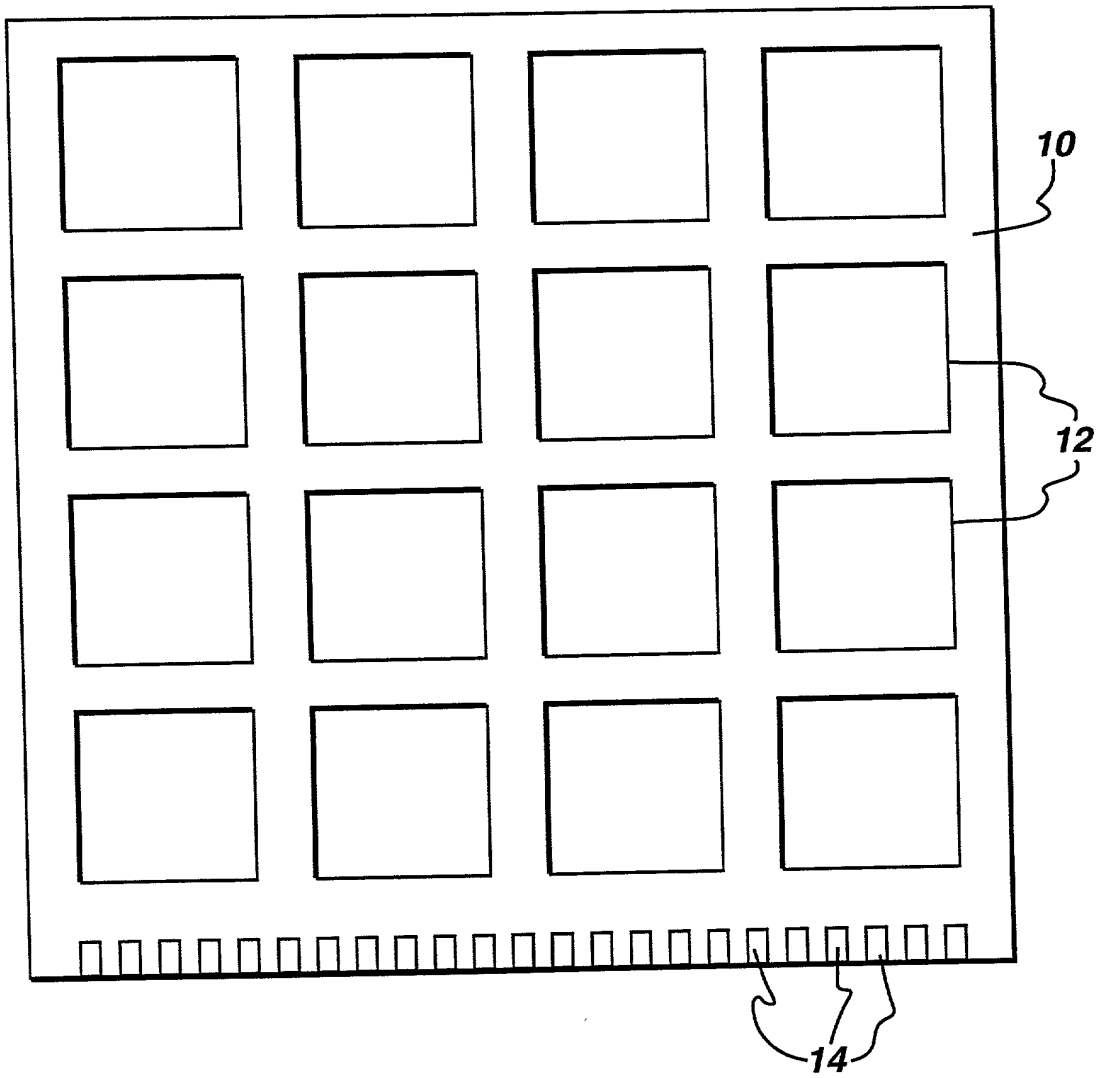

fig. 1

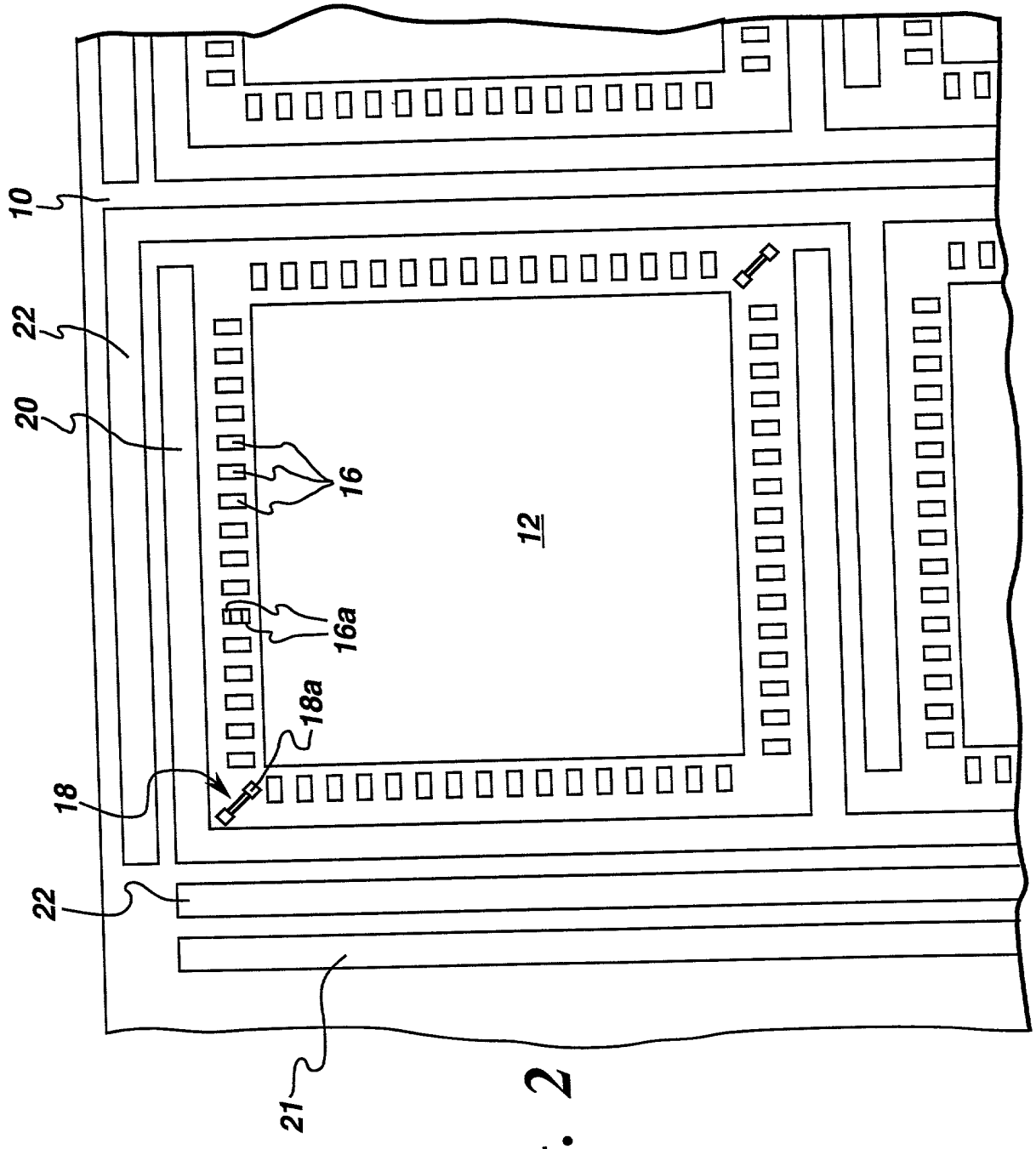

fig. 2

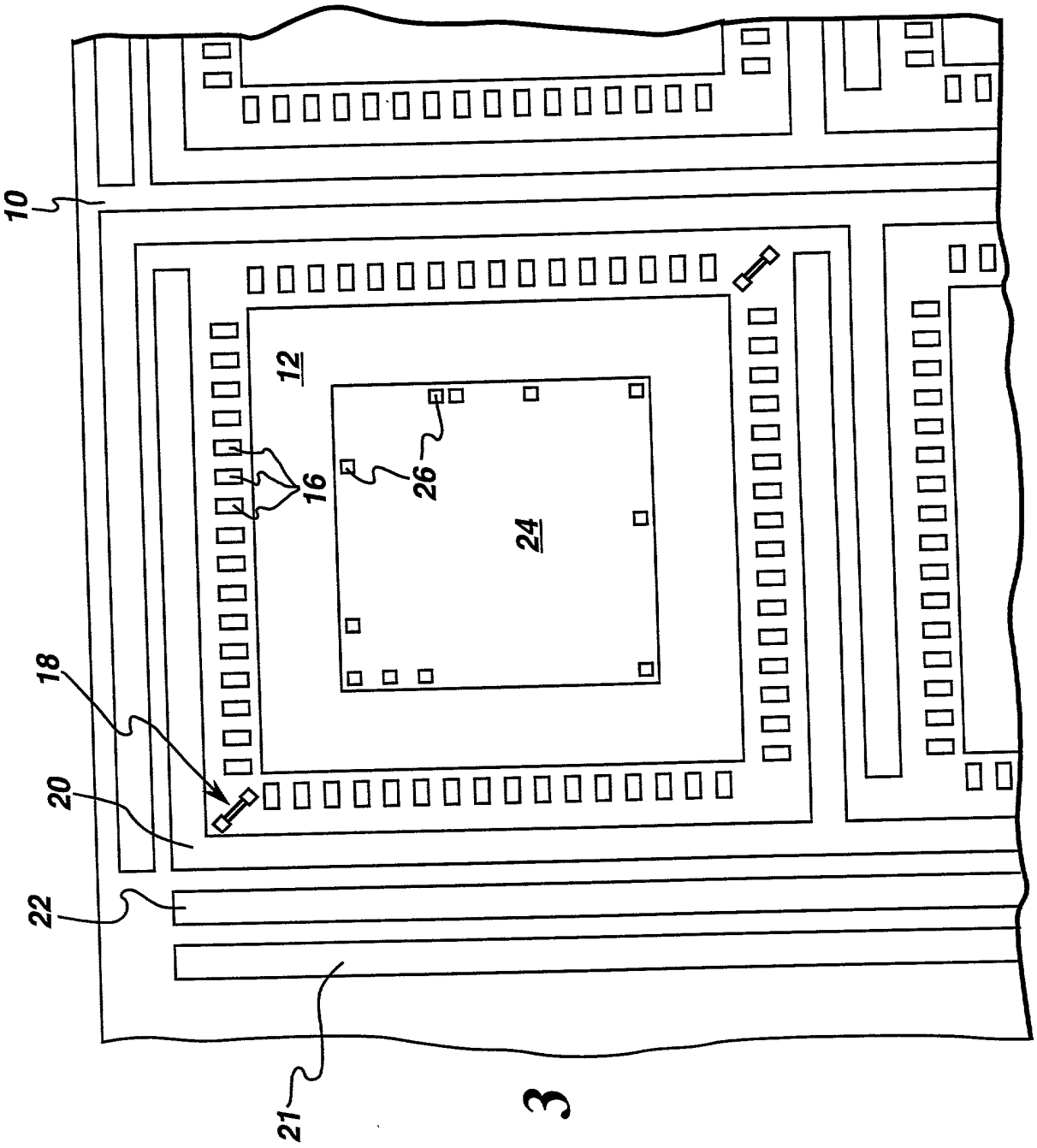

fig. 3

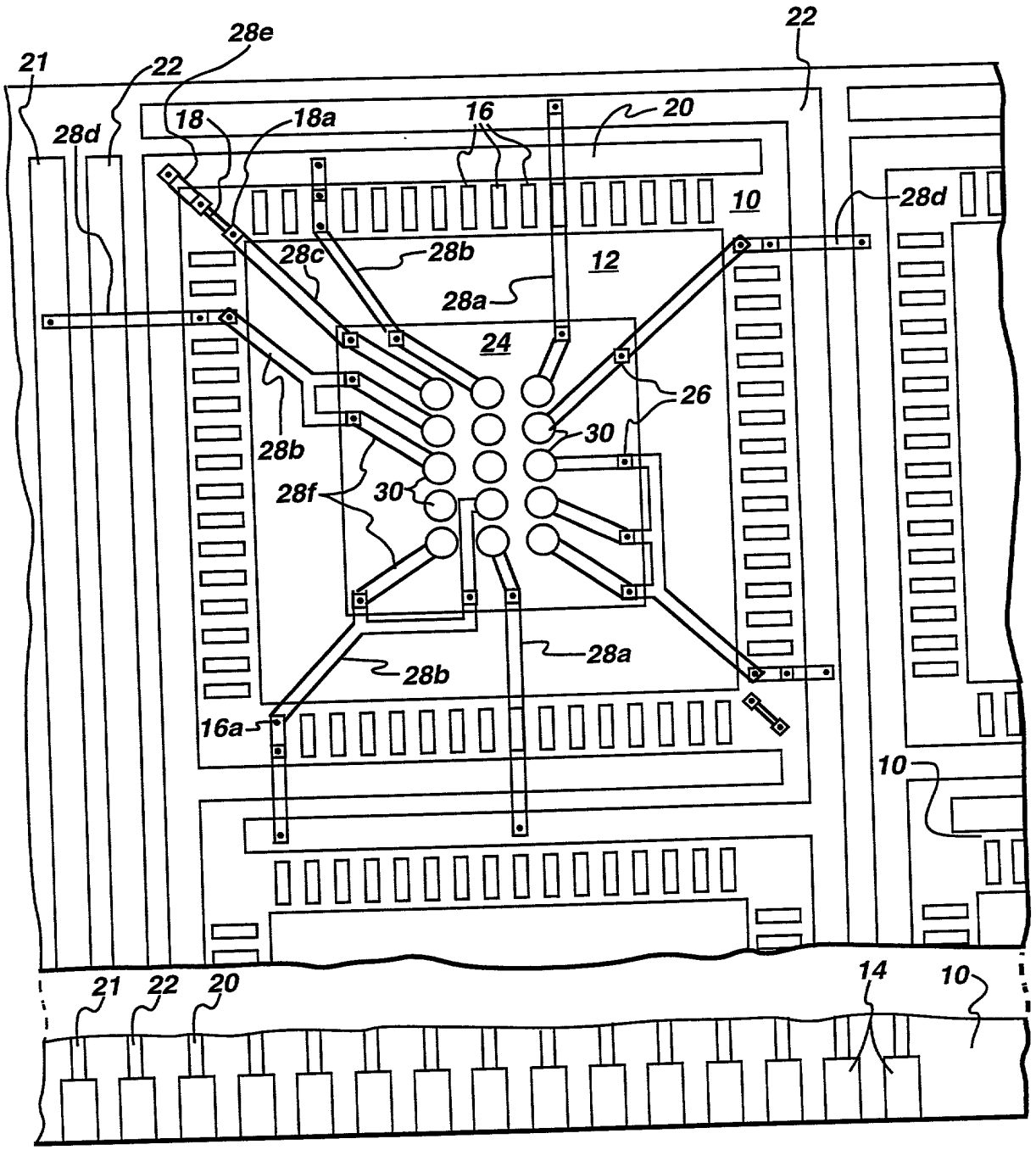
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fig. 4

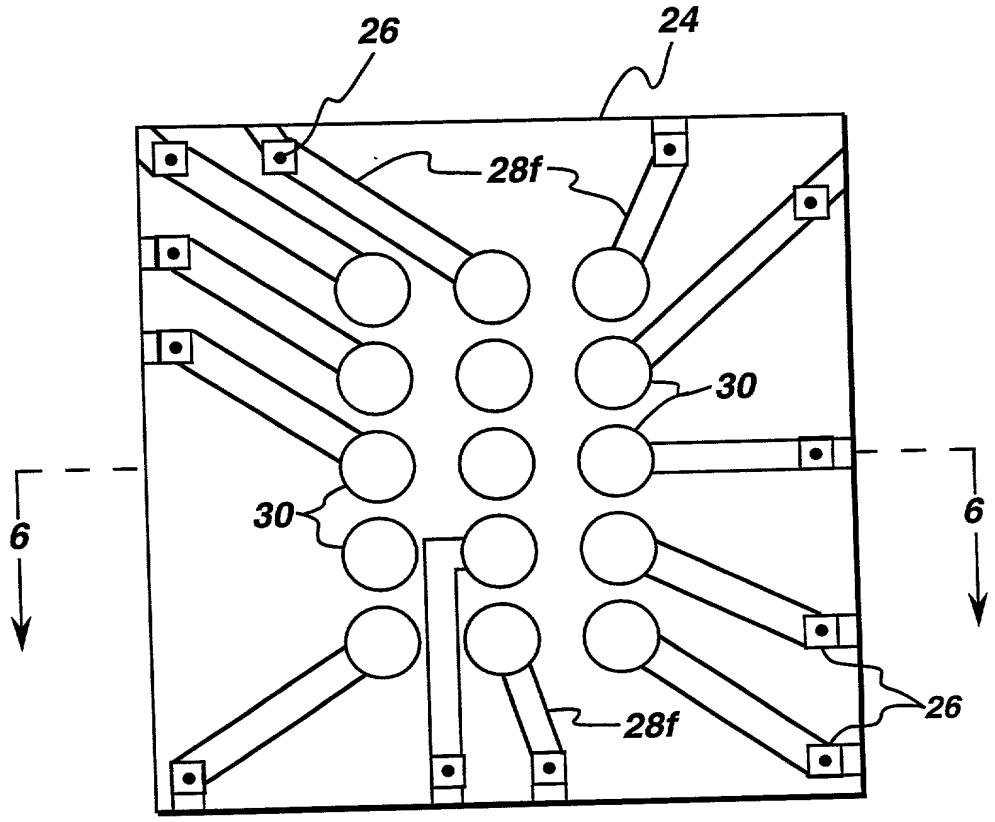


fig. 5

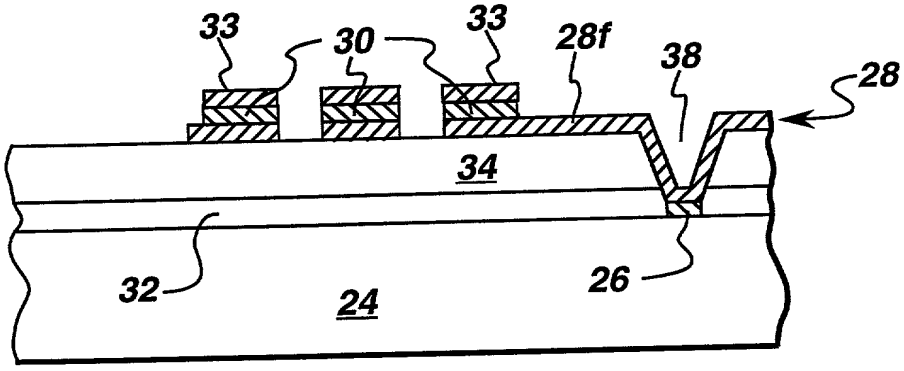
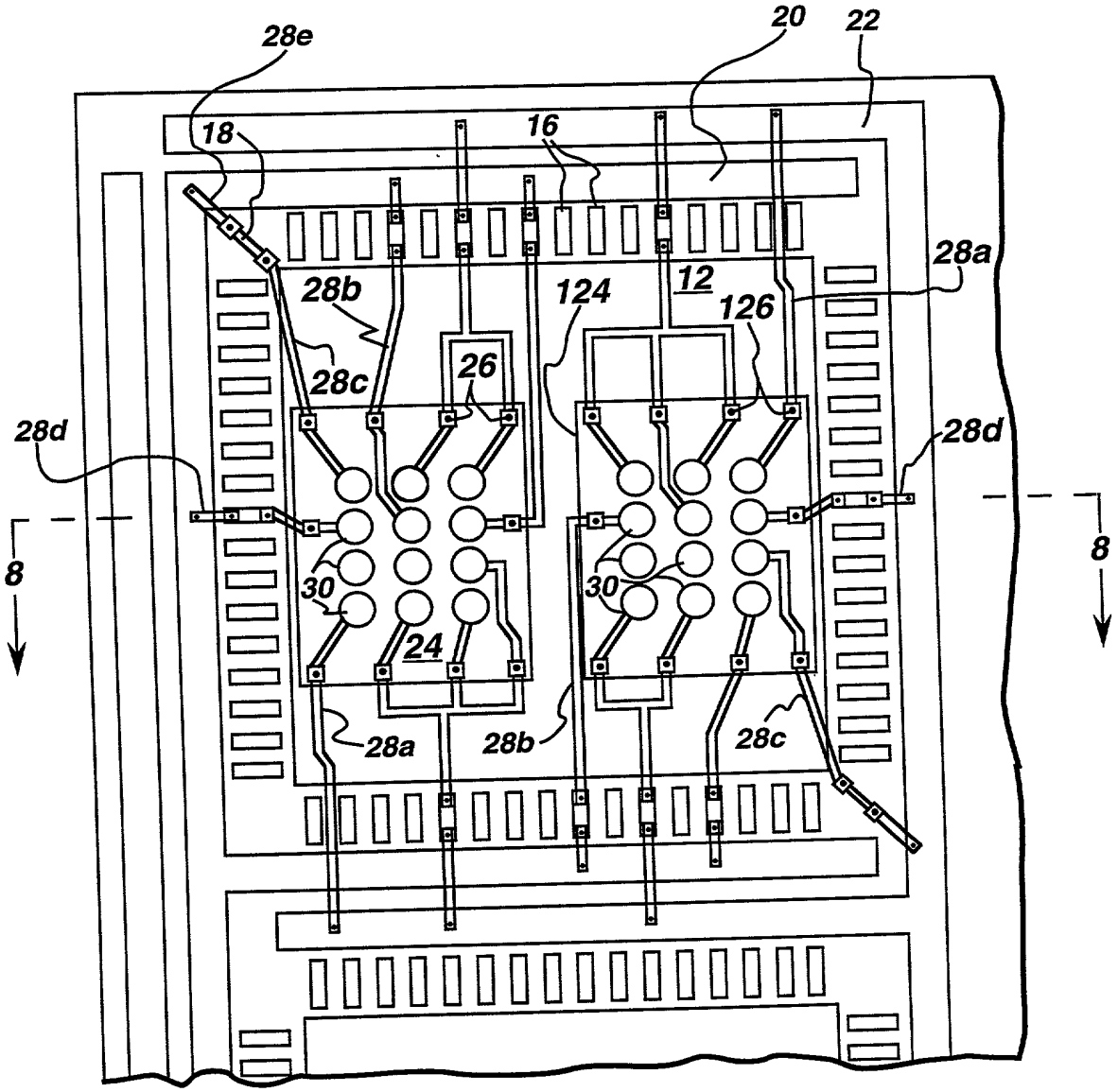


fig. 6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20
22
18
16
28a
28b
124
12
126
28c
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28d
8
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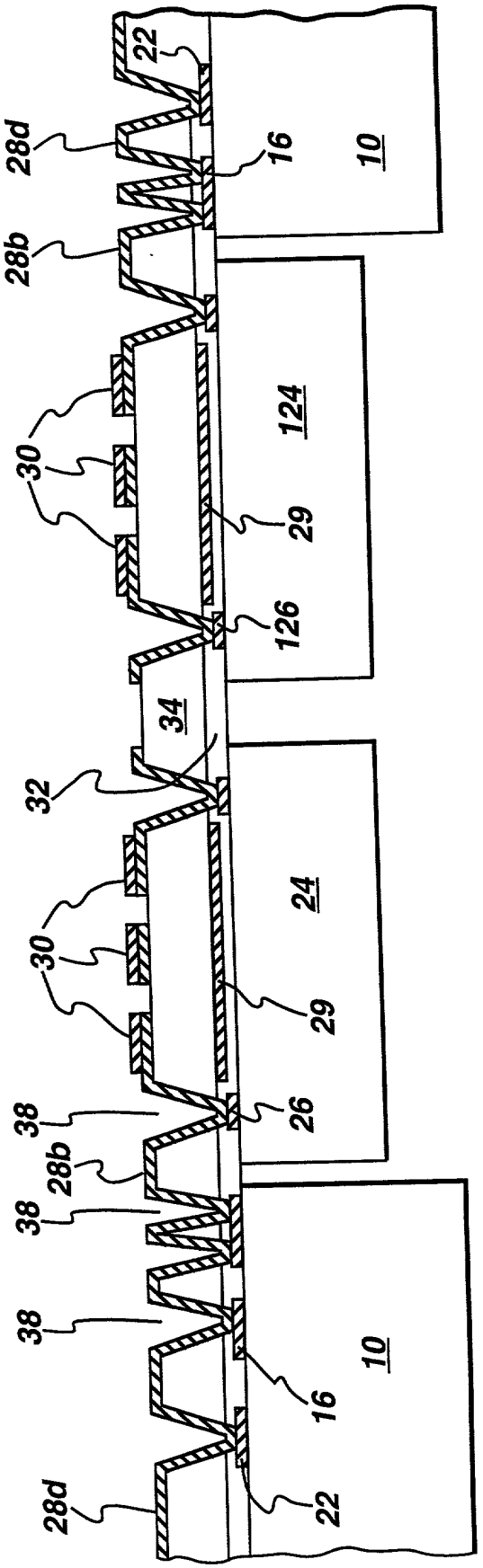
30
30
24
28a
28b
28c

fig. 7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10
28b
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28b
38
38
16
10
28d
22

fig. 8

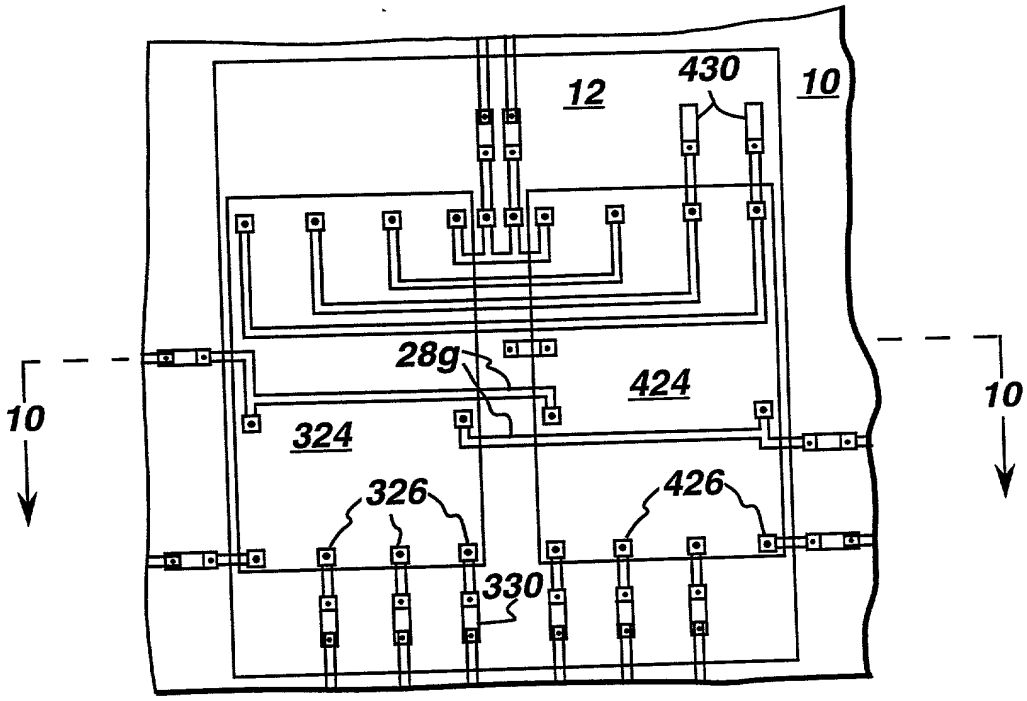

fig. 9

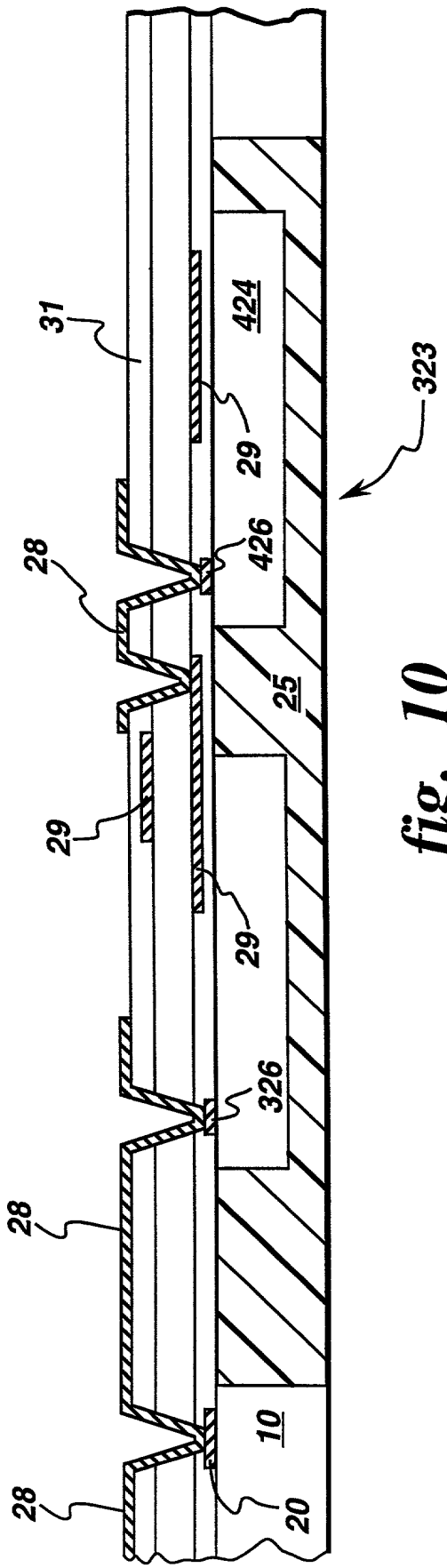

fig. 10

DE(ARATION FOR PATENT APPLIC/ ON

Docket Number
RD-24,889

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entited:

CHIP BURN-IN AND TEST STRUCTURE AND METHOD

the specification of which is attached hereto unless the following box is checked:

☐ was filed on as United States Application Number or PCT International Application Number _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(s) **Priority Claimed**

(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code §120 of any United States Application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith

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5/95

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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City and State

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Full name: _____
First Name Middle Name Last Name

Signature: _____ Date _____

Residence: _____ Citizenship: _____
City and State

Post Office Address: _____